REMARKS

The Examiner has rejected claims 13 and 15 under 35 USC 101 for being directed to non-statutory subject matter. In so doing, the Examiner refers explicitly to a computer program recitation. Within this context the applicant interprets the rejection of claim 15 to be in error, since that claim is not directed to a computer program, rather to a computer. It would appear that the Examiner intended to reject claim 14, which is also directed to a computer program. In response, thereto claims 13 and 14 have been cancelled.

Claims 1, 7, 9, and 13 through 16 stand rejected under 35 USC 102(e) as being anticipated by Fellman '702. Claims 3, 4 through 6, 11 and 12 stand rejected under 35 USC 103(a) as being unpatentable over Fellman in further view of Lehr '266.

The applicant respectfully disagrees with the 35 USC 102 rejections of independent claims 1 and 9 for the following reasons.

In particular, Fellman does not disclose a bus guardian having means for examining a synchroni**zed** clock signal using an internal clock signal, as recited in the independent claims. On the contrary, Fellman discloses a slave device (that is: a device adapter, see column 11 line 6) having a local clock 1010 which is less precise than a master clock forming a common time base. The local clock 1010 may be synchronized to the master clock (see column 10 lines 64-66). Therefore, it is the local clock 1010 which is a synchroni**zed** clock whereas the master clock constitutes a synchroni**zing** clock. For this reason, Fellman fails to disclose a synchroni**zed** clock signal *in addition* to a local clock 1010.

In order to provide some clarification, it is observed that Fellman (column 11 lines 6-15) refers to the local clock 1010, which is the same as the

clock 1010 of the processor 1000 (see Fellman fig. 3). However, there is no additional clock and accordingly the only clock to which the local clock 1010 can be synchronized is the master clock. However, the master clock is not a synchroni**zed** clock. Moreover, it is not the master clock signal that is examined, rather the local clock 1010. Therefore, Fellman fails to disclose an additional clock which is examined by a local clock 1010. In this manner, Fellman also fails to disclose a bus guardian having means for examining a synchroni**zed** clock signal using an internal clock signal. The anticipation rejection is therefore improper.

With respect to claim 2, it is observed that, since Fellman does not disclose any additional clock in the communication controller other than the local clock 1010, Fellman cannot disclose an additional clock signal as claimed. Accordingly, Fellman cannot disclose means for passing the additional clock signal to the bus guardian or means for monitoring the additional clock signal.

Claims 9, 16, 18 and 19 recite features corresponding to the features of claim 1 and therefore also not anticipated by Fellman.

Moreover, claims 2-8, 10-12, 17, and 18 are dependent on a respective independent claim and are therefore similarly distinguished from the prior art for the reasons given.

The applicant has provided argumentation in support of the allowability of independent claims 1 and 9. The dependent claims of record inherent the limitations of the base claim and are therefore similarly distinguished from the prior right of record for the reasons given. The applicant therefore respectfully requests favorable review by the US PTO and passage to issuance.

No new matter has been added to this amendment.

Respectfully submitted,

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